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Temperature dependence of the current–voltage characteristics of Sn/PANI/p-Si/Al heterojunctions

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Abstract

Sn/PANI/p-Si/Al heterojunctions were fabricated by electropolymerization of aniline on chemically cleaned p-Si substrates. Current–voltage characteristics of Sn/PANI/p-Si/Al heterojunctions measured in the temperature range 140–280 K are presented and analyzed. Although these devices were clearly rectifying, their I–V characteristics were non-ideal, which can be judged from the nonlinearity in the semi-logarithmic plots. The high values of the ideality factor n depending on the sample temperature may be ascribed to a decrease of the exponentially increasing rate in current due to space-charge injection into the PANI thin film at higher forward bias voltages. Careful analysis of the forward bias I–V characteristics on a log–log scale indicates that the space-charge-limited current (SCLC) conduction controlled by an exponential trap distribution above the valence band edge dominates the current transport in the PANI/p-Si diodes at high voltages. Furthermore, the PANI was characterized by using Fourier transform infrared (FTIR) and ultraviolet–visible (UV–vis) spectra.

1. Introduction

Conductor polymers are molecular analogs of inorganic semiconductors and metals. The electrical conductivity of these polymers can change from insulating to metallic by chemical or electrochemical doping, depending on the molecular structure of the conducting polymer and the nature of the dopants [1–7]. In the chemical polymerization process, monomers are oxidized by oxidizing agents or catalysts to produce conducting polymers [1–7]. The advantage of chemical synthesis is that it offers mass production at a reasonable cost. On the other hand, the electrochemical method involves the direct formation of conducting polymers with better control of polymer film thickness and morphology, which makes them suitable for use in electronic devices. Their adaptable electrical properties, ease of device fabrication,

diversity and potentially low cost provide a practical alternative to conventional inorganic semiconductors in the field of solid-state electronics [1–10]. The ability to prepare junctions with well-defined electrical properties is a key step towards the development of polymer-based solid-state electronic devices. Among various conducting polymers, polyaniline (PANI) has been investigated because of its attractive properties from the practical point of view, e.g. its relatively good environmental stability, the optimum conductivity and the ease of preparation [3, 8–10]. The behavior of electro-active polymers has been considered from the point of view of sensors [11–16], field-effect transistor applications [17, 18], and Schottky diodes [19–27].

Campos *et al* [16] have prepared a conducting organic polymer by the electrochemical polymerization method. They have calculated the junction parameters of the Au/polyaniline contacts from its current–voltage and capacitance–voltage characteristics. They have shown that the shifts in the I–V and C–V dependence of the diodes were measured with different concentrations of the methane gas for different time intervals. It is well known that the interaction of polymers with small gaseous molecules gives rise to changes in the electrical conductivity. Stable field-effect transistors (FETs) were fabricated using water-soluble self-acid-doped conducting polyaniline and sulfonic-acid-ring-substituted polyaniline [17]. These FETs have ideal source current–drain source voltage characteristics and their field-effect mobilities can reach 0.33 $cm^2\ V^{-1}\ s^{-1}$, which is close to those of the amorphous silicon inorganic transistors (0.1–1.0 $cm^2\ V^{-1}\ s^{-1}$) used extensively at present. Heterojunction-based organic semiconductor devices formed by an organic semiconductor grown on an inorganic semiconductor have been widely studied and investigated for their potential use in electronics [28–39]. Organic/inorganic semiconductor diodes may be sensitive probes that are useful for increasing the quality of devices fabricated using an organic semiconductor in establishing processes for minimizing surface states, surface damage and contamination which may ultimately change the quality of devices fabricated using the semiconductor [36–39]. Such studies [36–39] not only make inorganic semiconductor/organic film interfaces potentially relevant in the fabrication of Schottky-type diodes with well-defined or actively tunable barrier heights, but also in fundamental studies of electronic processes at semiconductor interfaces.

Analysis of the current–voltage (I–V) characteristics of the diodes obtained only at room temperature does not give detailed information about the charge transport process and about the nature of the barrier formed. In fact, it neglects many possible effects that cause non-ideality in the I–V characteristics of the diode and reduce the barrier height. The temperature dependence of the I–V characteristics gives a better picture of the conduction mechanism and allows one to understand different aspects that shed light on the validity of the various processes involved [40–42]. Some studies [35–38] have also focused on understanding and controlling key parameters such as the interface potential barriers. Organic/inorganic heterojunction diodes were fabricated by employing p-type Si and thin films of poly-*N*-epoxipropylcarbazole (PEPC) doped with tetracyanoquinodimethane (TCNQ) by Ahmed *et al* [34]. They [34] grew the PEPC films on Si wafers at room temperature under different gravity (g) conditions, and the current–voltage characteristics of the grown hybrid structures were evaluated as a function of temperature. Also, they [34] found that all samples are p–p isotype heterojunctions and the junctions fabricated at a high value of g showed rectifying properties as a function of device temperature. Charge transport through a thin organic film may be an electrode-limited process or a bulk-limited process [43]. Some studies [29–31, 37–39] have demonstrated that carrier transport in polymeric and non-polymeric organic films is space-charge-limited current (SCLC) and trap-charge-limited current (TCLC). Riad [44] has fabricated p-nickel phthalocyanine (NiPc) organic thin films onto a gold electrode by vacuum deposition. The electrical conductivity has been measured [44] both after exposure to oxygen for 10 days and

after annealing at temperatures up to 423 K. From current density–voltage characteristics under forward bias of organic thin films, it was found [44] to be due to space-charge-limited current controlled by a discrete trap level at lower voltage sections and by an exponential distribution of traps at higher voltage regions.

In this work, Sn/PANI/p-Si/Al heterojunctions were fabricated by electropolymerization of aniline on chemically etched p-Si substrates. The temperature dependence of the current–voltage (I–V) characteristics of the Sn/PANI/p-Si/Al heterojunctions was studied in an attempt to obtain detailed information about the transport mechanisms of the device.

2. Experimental procedures

The diodes were prepared using single surface mirror cleaned and polished (as received from the manufacturer) p-type Si wafers with (100) orientation and 5–10 Ω cm resistivity. The wafer was chemically cleaned using the RCA cleaning procedure (i.e., a 10 min boil in $NH_4 + H_2O_2 + 6H_2O$ followed by a 10 min boil in $HCl + H_2O_2 + 6H_2O$) [45]. Before ohmic contact was formed on the p-type Si substrate, the samples were dipped in dilute HF:H_2O (1:10) for about 30 s to remove any native thin oxide layer on the surface. Finally the wafer was rinsed in deionized water (purity up to 18.2 MΩ cm). The wafer was dried with high-purity nitrogen and was then inserted into the deposition chamber immediately. The ohmic contact was made by evaporating Al on the back of the substrate, followed by a temperature treatment at 570 °C for 3 min in flowing N_2 in a quartz tube furnace. The ohmic contact side of the p-Si substrate was used as an anode and its edges were carefully covered by silicon. Then the polished and cleaned front side of the substrate was exposed to the electrolyte by mounting it in an experimental set-up employed for electropolymerization. A Pt plate was used as a cathode in the experimental setup. The electrolyte was composed of 0.1 M monomer (aniline) and 1.5 M the HCl acid. Aniline (Merck) was distilled at reduced pressure just before the use and stored in the dark at low temperature. The polymer film was electrochemically deposited on the surface of the p-Si semiconductor in electrolyte solution under the conditions of a constant voltage of 0.7 V and at room temperature. The area of the circular polyaniline contacts on the p-Si was 7.1×10^{-2} cm^2. After polymerization was completed, the polyaniline-coated surface was rinsed in an acetonitrile–water mixture to get rid of the monomer and then carefully dried. Finally, to perform the electrical measurements a layer of Sn was deposited on the surface of the polyaniline films by the vacuum evaporation technique under a pressure of about 10^{-6} mbar. Thus, Sn/PANI/p-Si/Al heterojunctions were obtained. All evaporation processes were carried out in a vacuum coating unit at about 10^{-6} mbar. The current–voltage (I–V) characteristics of the devices were measured in the temperature range 140–280 K using a Leybold Heraeus closed-cycle helium cryostat that enables one to make measurements in dark conditions. The sample temperature was monitored by a copper–constantan thermocouple and a Windaus MD850 electronic thermometer with sensitivity better than ±0.1 K.

Furthermore, a Fourier transform infrared (FTIR) spectrum of the PANI was obtained by using a Perkin Elmer Spectrum BX FTIR system recorded between 400 and 4000 cm^{-1} with a 4 cm^{-1} resolution from KBr pellets. UV–vis spectra were recorded between 270–900 nm using a 1 cm path-length quartz cuvette and pure N, N-dimethylformamide (NMP) on a Perkin Elmer Lambda 20 UV–vis spectrophotometer.

3. Results and discussion

The FTIR spectrum of polyaniline (PANI) is given in figure 1. In the spectrum, the N–H stretching band is observed at 3441 cm^{-1}. The 1560 cm^{-1} band is the characteristic band

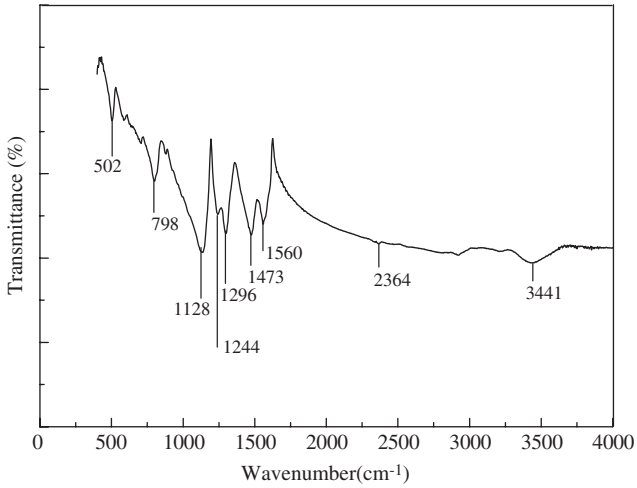

Figure 1. FTIR spectrum of the PANI.

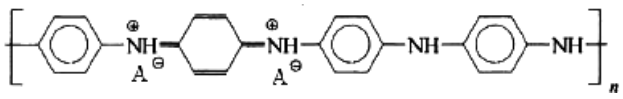

Figure 2. The emeraldine salt structure of the PANI. $A^- = Cl^-$; dopant anion.

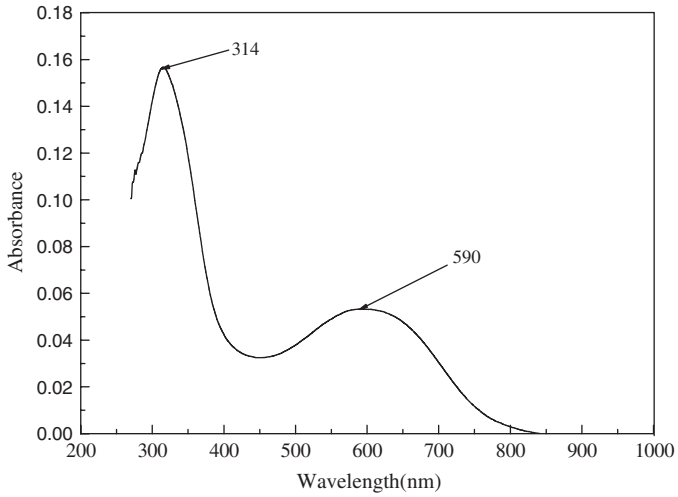

Figure 3. UV–vis spectrum of the PANI.

of the nitrogen quinone (Q) structure and 1473 cm^{-1} is related to the benzene ring (B) structure (figure 2). 1299 cm^{-1} and 1128 cm^{-1} correspond to the stretching peaks of C–N and C=N, respectively [46]. The 502 cm^{-1} band is related to C–H out-of-plane bending vibration. The UV–vis spectrum of PANI is shown in figure 3. It is clearly observed that the characteristic bands of polyaniline emeraldine salt structure are at 314 and 590 nm, which are attributed to $\pi \rightarrow \pi^*(\lambda_1)$, $n \rightarrow \pi^*$ (λ_2) transitions [47]. The general formula for ideal polyaniline (PANI) materials in their base forms consists of three benzenoid (–C_6NH_4–NH–)

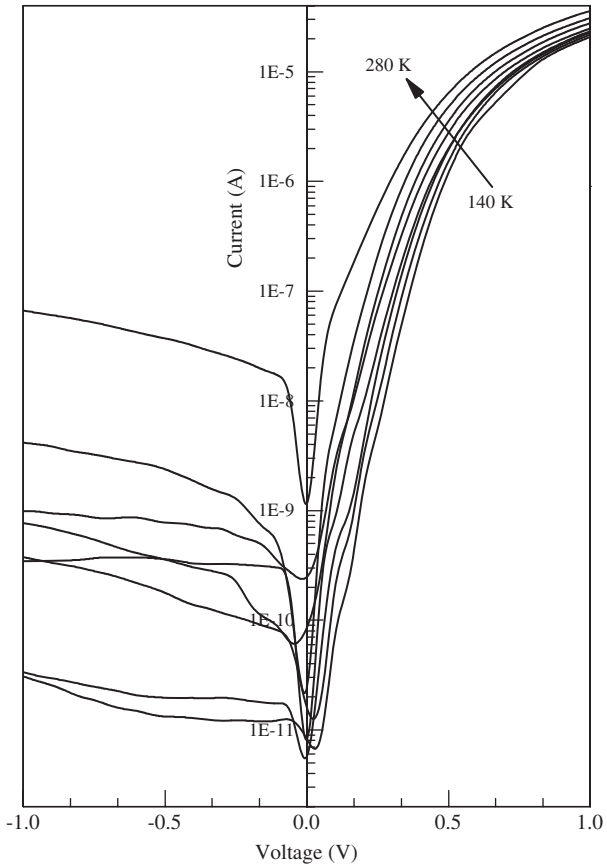

Figure 4. Experimental current–voltage characteristics of Sn/PANI/p-Si/Al heterojunctions in the temperature range 140–280 K.

units denoting B and one quinoid (–N=C_6H_4=N–C_6H_4) unit denoting Q, so they can be written as $[(B–B)_y(Q–B)_{1-y}]n$. The y value accounts for the oxidation state of the polymer: for example, leucoemeraldine (completely reduced, $y = 1$), emeraldine salt (half reduced, $y = 0.5$) and pernigraniline salt (completely oxidized, $y = 0$) states [48–50].

Figure 4 shows the experimental semi-logarithmic forward and reverse bias current–voltage (I–V) characteristics of the Sn/PANI/p-Si/Al heterojunctions for dc bias voltages in the temperature range 140–280 K. It shows an exponential increase in the forward current with applied voltage for the junction at low voltage range. This exponential dependence in the lower voltage range can be attributed to the formation of a depletion region between Si and the PANI thin film. In the forward bias condition, the ohmic contact made by evaporating on the back surface of the p-Si substrate was positively biased with respect to the Sn electrode (Schottky contact) on the PANI layer. That is, the thermionic emission over the PANI/p-Si contact is important at low current density. According to the thermionic emission theory for moderated doped semiconductors, the current–voltage relationship of a Schottky diode with a thin interfacial layer can be expressed by [51, 52]

$$I = I_o\left[1 - \exp\left(-\frac{qV}{kT}\right)\right]\exp\left(\frac{qV}{nkT}\right) \quad (1)$$

where V is the applied voltage, n is the ideality factor and is a measure of the conformity of the diode to pure thermionic emission, k is the Boltzmann constant, T is the absolute temperature, q is the electron charge, and I_o is the saturation current determined by [51, 52]

$$I_o = AA^*T^2 \exp\left[-q\frac{\Phi_{\mathrm{bo}}}{kT}\right] \tag{2}$$

where A is the diode area, A^* is the effective Richardson constant of 32 A cm^{-2} K^{-2} for p-type Si [52], and Φ_{bo} is the barrier height at zero bias.

The experimental values of the barrier height at zero bias Φ_{bo} and the ideality factor n are determined from intercepts and slopes of the forward-bias $\ln I$ versus voltage (V) plot according to the thermionic emission theory at each temperature, respectively. The values of the barrier height at zero bias and ideality factor have been changed from 0.423 eV and 3.085 at 140 K to 0.716 eV and 1.868 at 280 K, respectively. The very strong temperature dependence of the ideality factor and barrier height shows that the forward bias transport properties of the heterojunction diodes fabricated at high bias voltages are not well modeled only by the thermionic emission even when it was modified by the incorporation of a series resistance effect. The series resistance is the sum of the neutral bulk resistance and ohmic contact resistance. The numerical/graphical analysis of the current–voltage–temperature data of a real junction would become rather complicated or less physically informative if bulk conduction phenomena in the junction materials largely mask the actual junction-like behavior, particularly when at least one of its materials has a high temperature/voltage dependent inherent resistivity, as stated in [35, 37]. In principle, the effect of bulk conduction in a junction having a highly resistive semiconducting layer becomes important when the junction is at high bias voltages in the forward bias direction only and when it has a dominant rectifying junction-like behavior [35, 37]. This also seems plausible in the PANI/p-Si heterojunction used in the present work. Further, experimentally observed departures from the diode-like behavior of a real junction under high bias voltages and the consequent additional complication of a reliable analysis of its measured I–V–T data may also results from other conduction mechanisms related to the existence of some insulating interfacial layer, recombination–generation processes in the depletion regime and high injection levels [35, 51, 52].

Generally, the experimental isothermal current–voltage characteristics can be treated using an empirical relation of the form $I(V,T)\alpha \exp(eV/nkT)$. A careful examination of the measured I–V–T curves of the present heterojunction revealed that the behavior of their forward current at intermediate and high bias voltages cannot be reliably analyzed using such an empirical formula even when it is modified by the incorporation of a series resistance effect over a limited narrow bias region. These results imply that additional transport mechanisms are dominant in these devices. This suggests that conduction processes occurring in the highly resistive PANI layer of the Sn/PANI/p-Si/Al diode would be a possible alternative candidate in determining its forward current in the intermediate and high bias regimes beyond that of the low bias diode-like behavior. To understand more clearly the electrical properties of the PANI/p-Si heterojunction diode, its I–V characteristics were plotted on log–log scale. Figure 5 illustrates the forward bias $\log I$ versus $\log V$ plots of the Sn/PANI/p-Si/Al heterojunction diode at four different temperatures. As can be seen from figure 5, the double-logarithmic forward bias I–V plots show a good linearity in the range of 0.2–0.5 V, along with the best-fit power-law curve. The values of the power-law parameter, m, were calculated from the slope of the linear portions of the double-logarithmic I–V plots under forward bias of the PANI/p-Si heterojunction for each measurement temperature, in the temperature range 140–280 K. Figure 6 is a plot of the temperature-dependent exponent m from the power laws in the I–V characteristics versus reciprocal temperature, which is fitted by a straight line corresponding to $T_{\mathrm{c}} = 959$ K. As

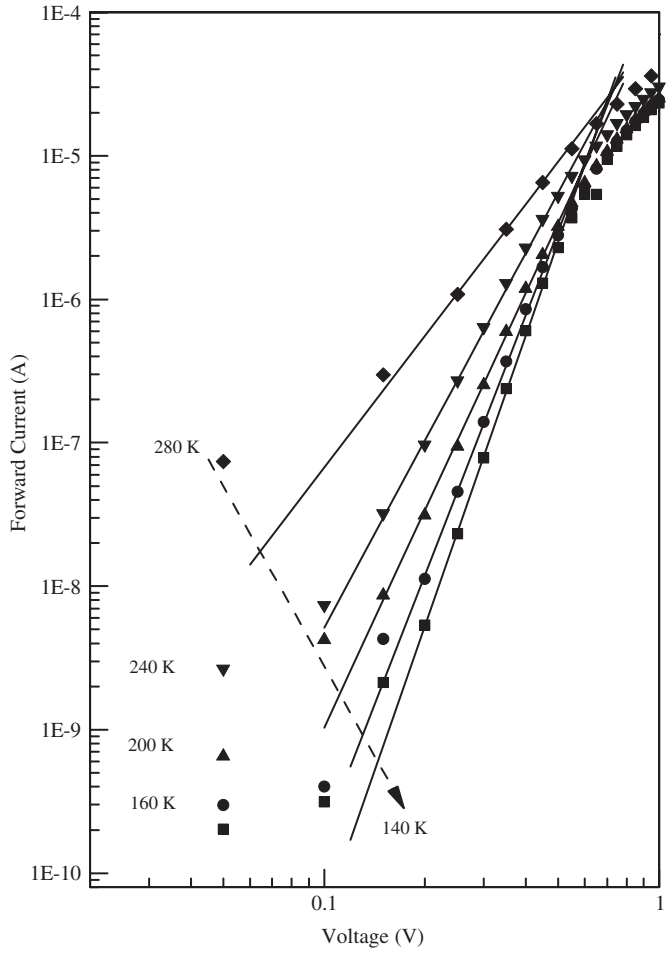

Figure 5. Experimental forward bias log I versus log V plot of the Sn/PANI/p-Si/Al heterojunction at five different temperatures from the plots given in figure 4.

can be seen from figure 6, the exponent m seems to increase with decreasing temperature, as expected for SCLC conduction [35, 37, 53–56]. This behavior can be used to derive the characteristic trap energy E_t from the temperature dependence of $E_t = kT_c$. At high applied voltage, the forward I–V characteristics in the temperature range 140–280 K are influenced by the transport properties of the highly resistive PANI layer [35, 37, 53–56]. That is, the shape of the I–V characteristics is not only controlled by the contacts, but strongly depends on the nature of the interfacial layer between the Sn electrode and the p-Si semiconductor. Generally, double-logarithmic forward bias I–V plots with a slope equal to or larger than 2 suggest the possibility of the space-charge-limited current (SCLC) mechanism [53–56]. The double-logarithmic forward bias I–V curves in figure 4 show a power-law behavior of the current, $I \propto V^{(m+1)}$, with different exponents $(m+1)$. That is, such power laws with exponents larger than two have been interpreted as an indication of trap-charge-limited conduction with an exponent trap distribution [53, 54]. The SCLC conduction should become important when the density of injected free-charge carriers is much larger than the thermally generated free-charge carrier density. In this study, the injected charge carriers can proceed through the junction from

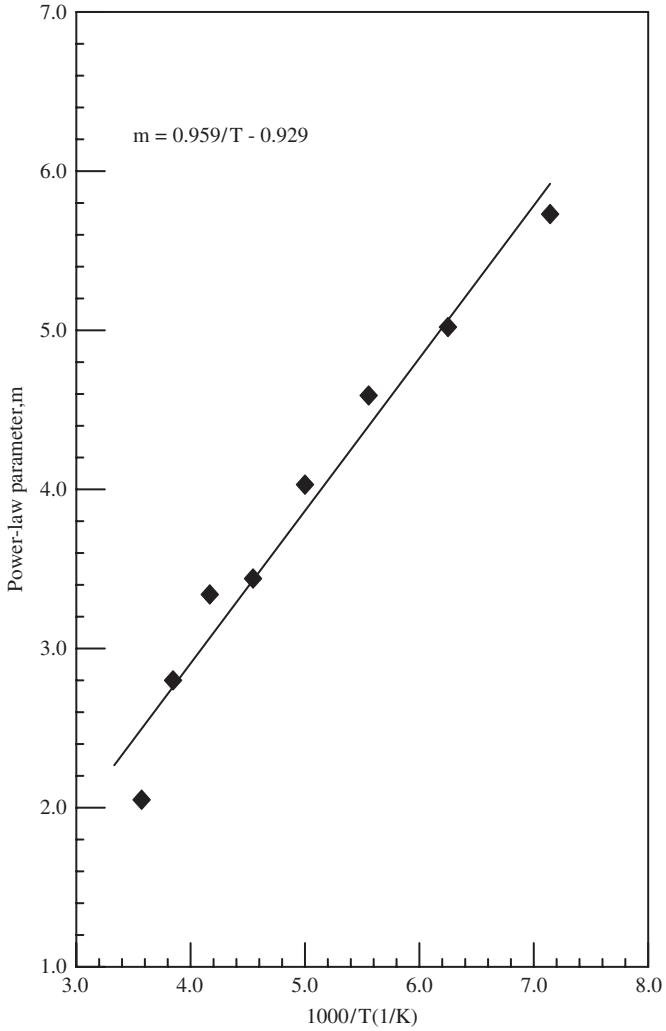

Figure 6. The power-law parameter m versus $1000/T$ plot. The solid lines indicate the fit to experimental data. Temperature dependence of the power-law exponents m obtained from the slope of the linear portions of the log I versus log V plot corresponding to each measurement temperature.

the moderately doped p-Si ($p \sim 4.5 \times 10^{15}$ cm^{-3}) into the highly resistive PANI material with much lower concentration of free holes to sustain a flow of trap-charge-limited current. Thus, it is possible to recognize the effect of traps on the conduction current which is dominated by an exponential distribution of traps at high voltage bias. Traps are locations arising from disorders, dangling bonds, impurities, etc, and are called localized states that very often capture free-charge carriers, playing a very important role in the conduction process of a polymer [34]. Similarly transport phenomena have been observed in dielectrics, amorphous semiconductors, wide band gap semiconductors, and other organic solids [33–39, 53–56].

The m versus $1000/T$ plot shows a linear dependence slope yielding a trap energy of about 0.08 eV from $E_t = kT_c$, and it can be said that most of the traps are deep traps as required by a E_t value of 0.08 eV. The characteristic energy obtained for our polyaniline film is 0.08 eV,

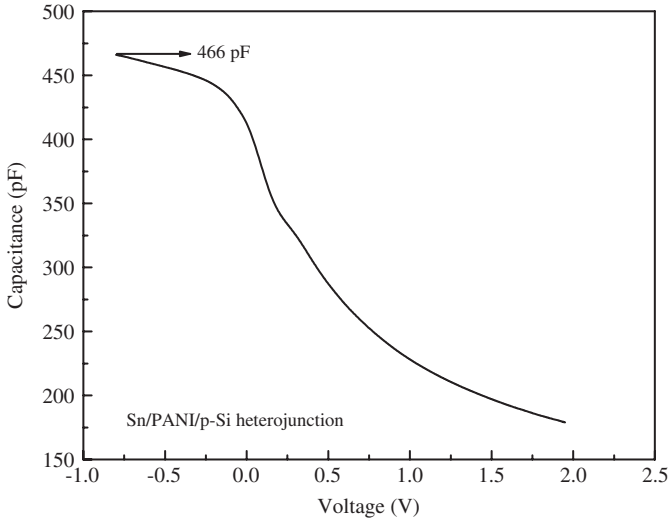

Figure 7. Experimental high-frequency capacitance–voltage plot of the Sn/PANI/p-Si/Al heterojunction at 296 K and 500 kHz.

comparable with the reported polyaniline emeraldine base (PANI-EB) films (0.11 eV) prepared by the solution-casting technique [57].

For the applied voltage above 0.2 V, the slope of $\log(J)$ versus $\log(V)$ plots are in the range of 2.05–5.83, which shows that the forward bias current is SCLC dominated by an exponential distribution of traps. The current density for this type of conduction is given by [35, 37, 53]

$$J = q\mu N_{\mathrm{v}}\left(\frac{\varepsilon\varepsilon_o}{qN_{\mathrm{t}}}\right)^m \frac{V^{m+1}}{d^{2m+1}} \tag{3}$$

where μ is mobility of holes in the PANI, N_{v} is the effective density of states in the valence band of the PANI, ε is the permittivity of the PANI film and is taken as 5.5 [28], ε_o is the permittivity of free space, $N_{\mathrm{t}} = P_o kT_{\mathrm{c}}$ [53] is the total concentration of traps. $P(E)$ is the trap concentration per unit energy range at an energy E above the valence band, and the exponential trap distribution can be expressed by [53]

$$P(E) = P_o \exp\left(-\frac{E}{kT_{\mathrm{c}}}\right) \tag{4}$$

where T_{c} is the characteristic temperature parameter of the trap distribution, T is the ambient temperature and d is the thickness of the PANI layer.

Figure 7 shows the capacitance–voltage plot of the Sn/PANI/p-Si/Al heterojunction at 500 kHz and 296 K. With high-frequency measurements, the measured value of the capacitance depends on the thickness of the polymer and inorganic p-Si layers and is given by $C^{-1} = C_{\mathrm{pol}}^{-1} + C_{\mathrm{Si}}^{-1}$ as expected for two layers in series [28, 31, 43, 57]. The capacitance increases towards high negative voltage and reaches the capacitance of the PANI layer alone. That is, the shape of the plot suggests charge accumulation at the PANI/p-Si interface and thus the capacitance of the PANI layer C_{pol} becomes important [37, 43, 57]. As can be seen from the C–V plot in figure 7, the value of C_{pol} is 466 pF. Using the geometrical relationship $C_{\mathrm{pol}} = \varepsilon A/d$ with the device area A ($=7.1\times10^{-2}$ cm^2) and the permittivity ε, we can calculate the PANI layer thickness, d, for the heterojunction using high-frequency C–V characteristics. Thus, the PANI layer thickness was calculated as 742 nm.

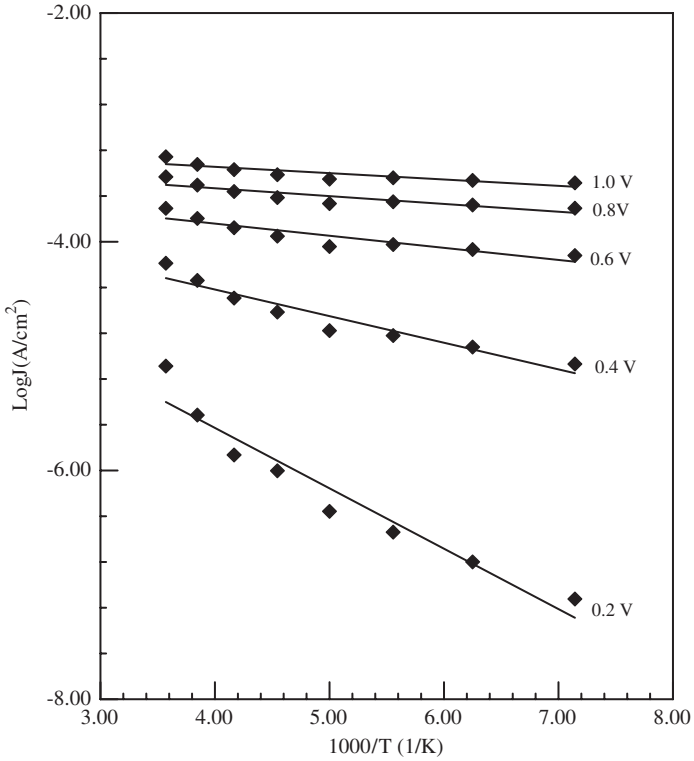

Figure 8. Experimental forward bias log(J) versus 1000/T plot at five different voltages obtained from figure 4 in the temperature range 140–280 K. The solid lines indicate the fit to experimental data.

Figure 8 also shows the variation of log (J) with 1000/T in the SCLC region, which gives a straight line. As can be seen from figure 8, the slope of the forward log J versus 1000/T plots decreases with increasing bias voltage; that is, the curves exhibit an electric field-dependent linearity [43, 58, 59]. The slope of the line presented in the log (J) versus 1/T plots is given by [30, 37, 44]

$$\frac{\mathrm{d}(\log J)}{\mathrm{d}(1/T)} = T_\mathrm{c} \log \frac{\varepsilon V}{q d^2 N_\mathrm{t}(E)}. \tag{5}$$

From equation (5), the total concentration of the trap can be calculated. The intercept on the log (J) axis in the log (J) versus 1/T plots is given by [30, 37, 44]

$$\log J = \log\left(\frac{q\mu N_\mathrm{v} V}{d}\right) \tag{6}$$

where J reveals the current density at infinite temperature ($1/T = 0$), and then μ can be determined from its value. The log(J) versus 1000/T plot at 1.0 V bias voltage in figure 8 has a slope of 55 A K cm^{-2} and an intercept of 3.123 A cm^{-2} in the temperature range 140–280 K. The values of $N_\mathrm{t} = 1.842 \times 10^{14}$ cm^{-3}, $\mu = 4.448 \times 10^{-6}$ cm^2 V^{-1} s^{-1} and $P_o = 5.854 \times 10^{15}$ cm^{-3} eV^{-1} for the PANI were calculated using equations (3)–(6) and $N_\mathrm{t} = P_o k T_\mathrm{c}$. The experimental values of the total trap concentration and the hole mobility of the conducting polymer PANI are determined from intercepts and slopes of the log(J) versus 1000/T plot at each bias voltage, respectively and using $N_\mathrm{t} = P_o k T_\mathrm{c}$, as given in table 1. As

Table 1. The experimental parameters obtained for the Sn/PANI/p-Si/Al heterojunction diode in the temperature range 140–280 K. $T_c = 959$ K.

V (V)	N_t (cm^{-3})	μ (cm^2 V^{-1} s^{-1})	P_o (cm^{-3} eV^{-1})
0.2	3.110×10^{13}	8.152×10^{-6}	3.761×10^{14}
0.4	1.263×10^{14}	4.043×10^{-6}	1.527×10^{15}
0.6	2.570×10^{14}	2.642×10^{-6}	3.108×10^{15}
0.8	3.755×10^{14}	1.889×10^{-6}	4.539×10^{15}
1.0	4.842×10^{14}	1.448×10^{-6}	5.854×10^{15}

can be seen from table 1, the average mobility value of the PANI is smaller than that given for polymeric thin films [58]. The mobility value in conjugated polymers is found to be around 10^{-4} cm^2 V^{-1} s^{-1} and it is known to depend on field and temperature [58–60]. As mentioned by [34], the mobility of free carriers reduces in the presence of traps. Therefore, the effective mobility will be smaller than the ideal case mobility for a given organic material. It has been shown that the experimental I–V–T characteristics of a device may be used to determine the electrical parameters of a conducting polymer by employing its different regions of operation.

4. Conclusions

Sn/PANI/p-Si/Al heterojunctions were fabricated by the electropolymerization of aniline on chemically cleaned p-Si substrates. A rectifying contact was formed between p-Si and Sn by means of the interfacial polyaniline layer. At lower voltages, the current–voltage characteristics of the diodes have an exponential dependence on voltage as a function of temperature. The forward bias I–V characteristics of the conducting polymer polyaniline interfaced to the p-Si have been explained by using the space-charge-limited current density model dominated by an exponential distribution of traps at high voltages. The bulk parameters of the PANI film, which is a good candidate for the active part of electronic devices, were calculated using current–voltage–temperature characteristics of the heterojunction.

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